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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,403	01/06/2004	Katsuhiro Kato	OKI.439D	3187

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,403	KATO, KATSUHIRO	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/305,954.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 12-14, 22-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Ker, Patent No. 6,075,686. With respect to claims 12 and 22, applicant's prior art (Fig. 14 and Fig. 15) teaches an electrostatic-breakdown-preventive and protective circuit for a semiconductor device which comprises a first power-source line 21 and a first ground line 22 for supplying bias to a first internal block 20; a second power-source line 31 and a second ground line 32 for supplying bias to a second internal block 30; a third power-source line 11 and a third ground line 12 for supplying bias to an input/output circuit portion 103; a protective transistor 10 disposed between the third power-source line 11 and the third ground line 12; and a connection line 25 for transferring an output signal of the first internal block 20 as an input signal of the second internal block 30.

However, the prior art fails to teach or suggest at least one of a first protective transistor provided between the first power-source line and the second power-source line and a second protective transistor provided between the first ground line and the second ground line, wherein at least one of the first

protective transistor and the second protective transistor is disposed in a vicinity of the connection line.

Ker teaches an ESD protection circuit for mixed mode integrated circuits with separated power pins. Ker discloses at least one of the a first protective transistor 410 provided between the first power-source line VDD and the second power-source line VDDA and a second protective transistor 420 between the first ground line VSS and the second ground line VSSA, wherein at least one of the first protective transistor 410 and the second protective transistors 420 is disposed in vicinity of the connection line as disclosed in Col. 7, lines 64-66 and Fig. 14.

Both teaching are related by being ESD prevention protective circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker, which teaches a first protective transistor and a second protective transistor, into the circuit of applicant's acknowledged prior art to create a circuit capable of bridging one available power supply to a second available power supply in order to drain excess energy from whichever supply had an abnormally high voltage level into the one with a normal voltage level.

With respect to claims 13 and 23, applicant's prior art teaches that the first 22, second 32 and third 12 ground lines are connected to a ground pad as disclosed in Fig. 15. Ker teaches that the second protective transistor 420 is

provided between the first ground line VSS and the second ground line VSSA as disclosed in Fig. 14.

With respect to claims 14 and 24, applicant's prior art teaches that the first 21 and second 31 power-source lines are respectively connected to power-source pads, and the power-source pads supplying differential potential level to the first and second power-source lines as disclosed in Fig. 15.

With respect to claim 26, applicant's prior art teaches that the third protective element 10 is a transistor as disclosed in Fig. 15. Ker teaches that the first protective element 410 and the second protective element 420 are protective transistors as disclosed in Fig. 14.

2. Claims 15-17, 25 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Ker, Patent No. 6,075,686 as applied to claims 12-14, 22-24 and 26 above, and further in view of Takasu, Patent No. 6,489,662. With respect to claims 15 and 25, the acknowledged prior art and Ker teaches the semiconductor device having the electrostatic-breakdown-preventive and protective circuit but does not disclose that the semiconductor device is formed on a SOI substrate. Takasu teaches a semiconductor device having a semiconductor integrated circuit formed on an SOI substrate as disclosed in Col. 2, lines 29-33.

All three teaching are related by being semiconductor devices having an ESD protecting circuit to prevent electrostatic breakdown. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to combine the teachings of Takasu, which teaches a semiconductor device formed on an SOI substrate, into the circuit of applicant's acknowledged prior art modified by Ker so that the semiconductor device is strong against ESD breakdown and cracking, breakage, etc., are prevented in a dicing process.

With respect to claims 16-17 and 27-28, the method of fabrication of transistors on SOI substrate described represents conventional practice in the art and as such does not represent any new inventive information. Ker teaches a transistor with gate oxides as disclosed in Col. 3, lines 51-56.

3. Claims 18-20 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Kato, Patent No. 6,515,337. With respect to claim 18, applicant's prior art (Fig. 14 and Fig. 15) teaches an electrostatic-breakdown-preventive and protective circuit for a semiconductor device, which comprises a first power-source line 21 and a first ground line 22 for supplying bias to a first internal block 20; a second power-source line 31 and a second ground line 32 for supplying bias to a second internal block 30; a third power-source line 11 and a third ground line 12 for supplying bias to an input/output circuit portion 103; a protective transistor 10 disposed between the third power-source line 11 and the third ground line 12; and a connection line 25 for transferring an output signal of the first internal block 20 as an input signal of the second internal block 30.

However, the prior art fails to teach or suggest at least one of a first resistor one end of which is connected to the first power-source line and another

end of which is connected to the second power-source line, and a second resistor one end of which is connected to the first ground line and another end of which is connected to the second ground line.

Kato teaches an electrostatic destruction prevention protection circuit. Kato discloses at least one of a first resistor 60 one end of which is connected to the first power-source line 100 and another end of which is connected to the second power-source line 200, and a second resistor 70 one end of which is connected to the first ground 3 and another end of which is connected to the second ground line 300, wherein at least one of the first resistor 60 and the second resistor 70 is disposed in a vicinity of the connection line 9 as disclosed in Fig. 1.

Both teaching are related by being electrostatic prevention protective circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kato, which teaches a first and a second resistor, into the circuit of applicant's acknowledged prior art to create a circuit capable of bridging one available power supply to a second available power supply in order to drain additional (the resistor will cause heat to be created, which aids in lowering an ESD event) excess energy from whichever supply had an abnormally high voltage level into the one with a normal voltage level.

With respect to claim 19, applicant's prior art teaches that the first 22, second 32 and third 12 ground lines are connected to a ground pad as disclosed

in Fig. 15. Kato teaches that the second resistor 70 is provided between the first ground line and the second ground line as disclosed in Fig. 1.

With respect to claim 20, applicant's prior art teaches that the first 21 and second 31 power-source lines are respectively connected to power-source pads, and the power-source pads supplying differential potential level to the first and second power-source lines respectively as disclosed in Fig. 15.

With respect to claim 29, Kato teaches that the first 60, second 70 and third 20 protective elements are resistors as disclosed in Fig. 1.

4. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Kato, Patent No. 6,515,337 as applied to claims 18-20 above, and further in view of Takasu, Patent No. 6,489,662. With respect to claim 21, the acknowledged prior art and Kato teaches the semiconductor device having the electrostatic-breakdown-preventive and protective circuit but does not disclose that the semiconductor device is formed on a SOI substrate. Takasu teaches a semiconductor device having a semiconductor integrated circuit formed on an SOI substrate as disclosed in Col. 2, lines 29-33.

All three teaching are related by being semiconductor devices having an ESD protecting circuit to prevent electrostatic breakdown. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Takasu, which teaches a semiconductor device formed on an SOI substrate, into the circuit of applicant's acknowledged

prior art modified by Kato so that the semiconductor device is strong against ESD breakdown and cracking, breakage, etc., are prevented in a dicing process.

5. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
11/16/2005

PHUONG T. VU
PRIMARY EXAMINER